Single Event Effects (SEE) Testing of Embedded DSP Cores within Microsemi RTAX4000D Field Programmable Gate Array (FPGA) Devices

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Outline

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- **Device under test**
- **Design of test structure**
- **Test setup**
- **Test results**
- **Conclusions**

To be presented by Chris Perez at the Revolutionary Electronics in Space (ReSpace) / Military and Aerospace Programmable Logic Devices (MAPLD) 2011 Conference, Albuquerque, NM, August 22-25, 2011, and to be published on nepp.nasa.gov web site.
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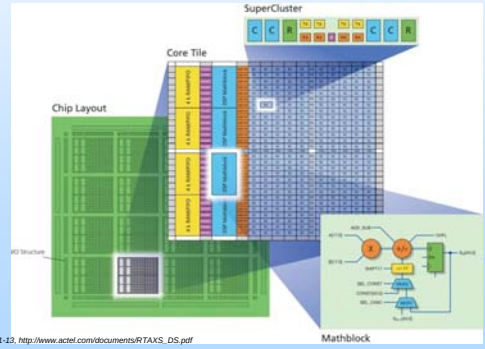
Motivation

- Accurately characterize DSP core single-event effect (SEE) behavior
- Test DSP cores across a large frequency range and across various input conditions
- Isolate SEE analysis to DSP cores alone
- Interpret SEE analysis in terms of single-event upsets (SEUs) and single-event transients (SETs)
- Provide flight missions with accurate estimate of DSP core error rates and error signatures

Device Under Test

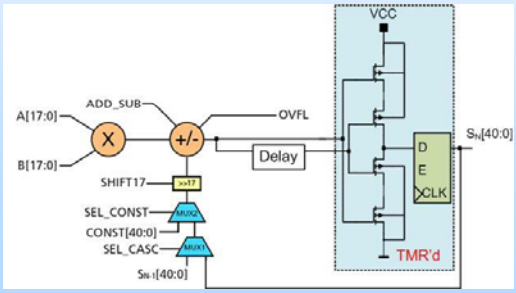
- Microsemi RTAX-DSP FPGAs
  - 0.15 µm CMOS logic fabric with anti-fuse configuration technology
  - Embedded multiply-accumulate DSP blocks
  - Sequential cells SEU-hardened via TMR and output buffer triple-drive



Source: Figure 1-13, http://www.actel.com/documents/RTAXS_DS.pdf

DSP Blocks

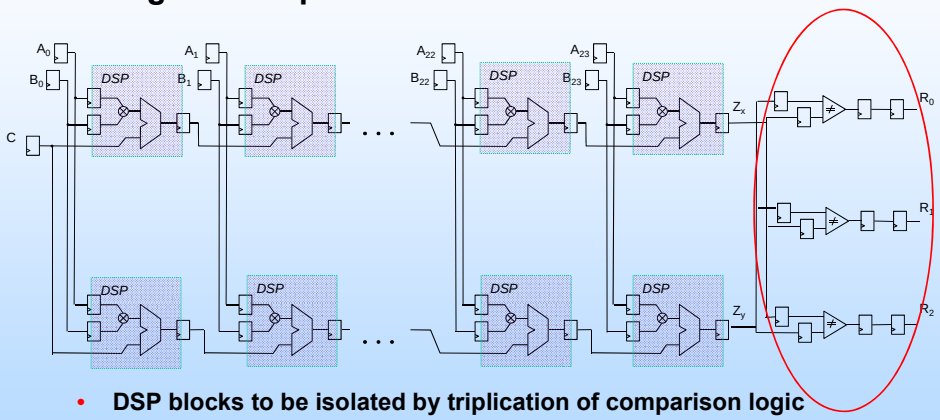
- 18x18 bit multiplier with 41-bit accumulator
- Option to register inputs and ouputs for up to 125 MHz operation
- Configure as one 18x18 multiplier or two 9x9 multipliers
- Cascading, arithmetic shift, and feedback capabilities
- SEU hardened by TMR of input and output registers
- SET mitigated by guard-gate at output of combinatorial logic with delay chain set to 750 ps delay



Source: IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 57, NO. 6, DECEMBER 2010, pp. 3537-3546

Test Structure

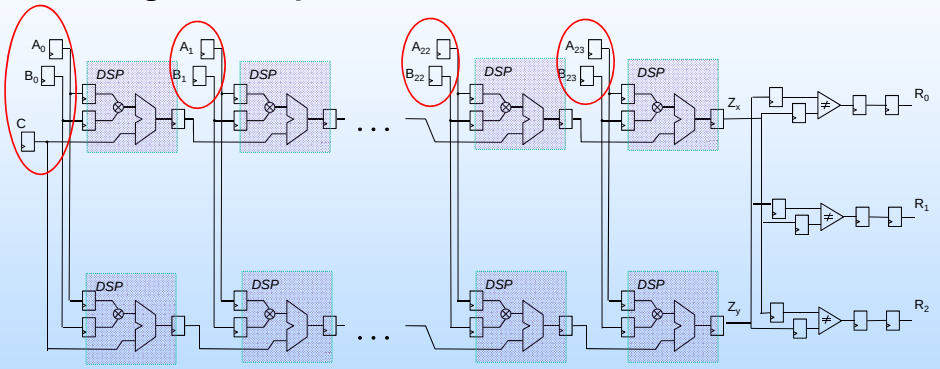
Design of one pair of DSP chains



- DSP blocks to be isolated by triplication of comparison logic
  - *Eliminate SETs/SEUs contributed from other logic*

Test Structure

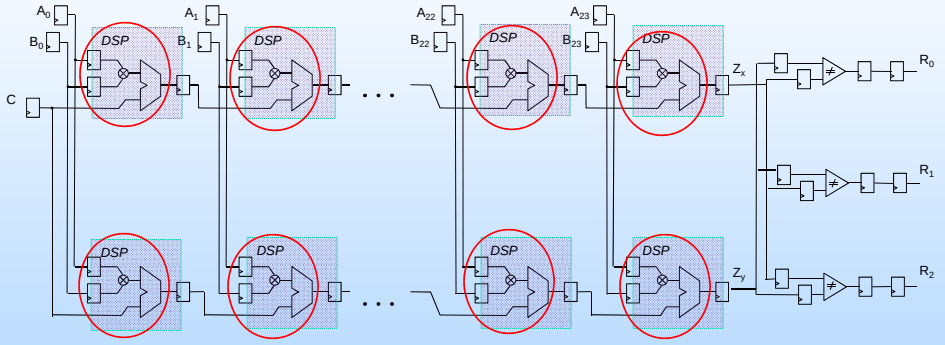
Design of one pair of DSP chains



- **Test across all frequencies and input conditions**
  - *Frequencies up to 120 MHz, stimulating all possible input cases*

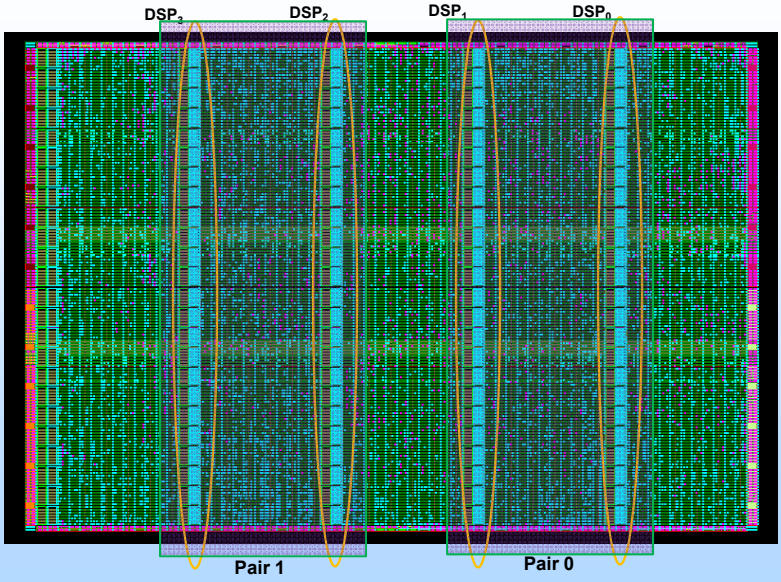
Test Structure

Design of one pair of DSP chains

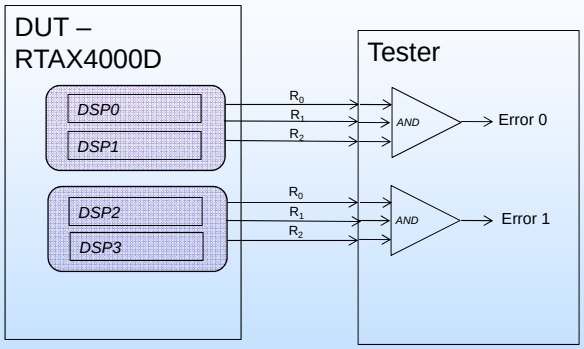


- **Enable multiplier AND adder modes, with cascading and pipelining of DSP outputs**
  - *Maximize SEE visibility when using as multiplier AND adder instead of as multiplier without adder or adder without multiplier*

Test Structure



Test Setup

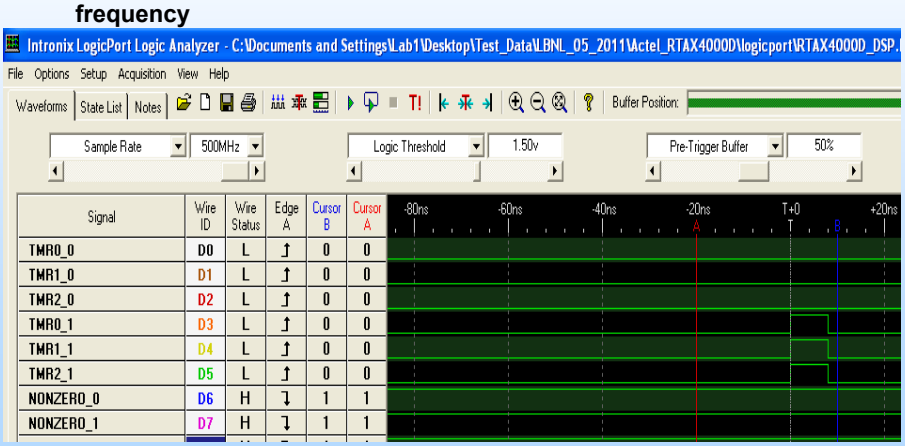


Error Conditions

- SEU in any DSP block within a chain results in single-cycle upset at output of that chain
- Assume Z_x, Z_y are outputs of paired chains
  - If Z_x /= Z_y, then within last 24 cycles, SEU occurred in one of 24 DSPs in chain *X* or in chain *Y*
  - Comparison logic for Z_x, Z_y is triplicated, producing output flags R_0, R_1, R_2 all set high when Z_x /= Z_y
- Flags R_0, R_1, R_2 are compared in tester, and when all set high, SEU detected in one of 48 DSPs within pair
- All other outcomes of R_0, R_1, R_2 are ignored as they don't represent SEUs in DSPs

Example DSP Upset

- Logic analyzer screenshot of actual SEU in DUT DSP cores captured by tester system
- Sampling clock is 2X frequency of maximum DSP operating frequency



Test Setup

- A_i, B_i, C are all selected by separate 2-bit inputs
  - 00 selects 0
  - 01 selects +1
  - 10 selects -1
  - 11 selects a counter
- For first round of testing, A_i, B_i set to counter for all cases, C remained variable
- Test matrix:

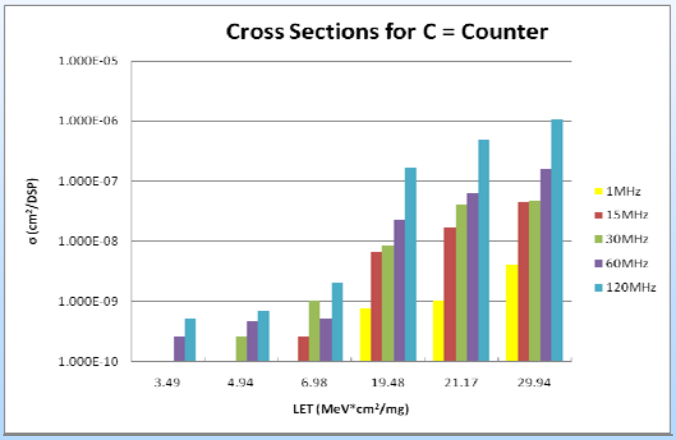
1 MHz C=0	15 MHz C = 0	30 MHz C = 0	60 MHz C = 0	120 MHz C = 0
1 MHz C = +1	15 MHz C = +1	30 MHz C = +1	60 MHz C = +1	120 MHz C = +1
1 MHz C = -1	15 MHz C = -1	30 MHz C = -1	60 MHz C = -1	120 MHz C = -1
1 MHz C = count	15 MHz C = count	30 MHz C = count	60 MHz C = count	120 MHz C = count

Test Parameters

- Heavy Ion Testing at LBNL
  - Energy : 15 MeV
  - Fluence : up to 4.0E+7, OR until significant number of upsets observed
  - Fluxes
    - 2.0E+5 to 2.3E+5 : Ne
    - 9.7E+4 to 1.1E+5 : Ar
    - 7.0E+4 to 1.0E+5 : Cu
  - Angles of incidence tested : 0°, 45°, and 60°
  - Effective LETs tested : 3.94 to 29.94 MeV·cm^2/mg

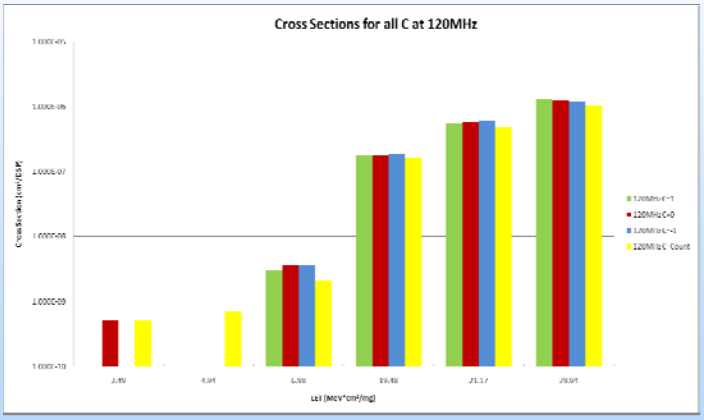
Test Results

- Individual upset counts normalized by total number of DSP blocks
- Upset counts reported by tester across frequencies
- This shows effect of frequency on error rate



Test Results

- Cross section for all cases of C input at 120 MHz (worst-case)
- Choice of C input does not appear to have significant effect on cross section



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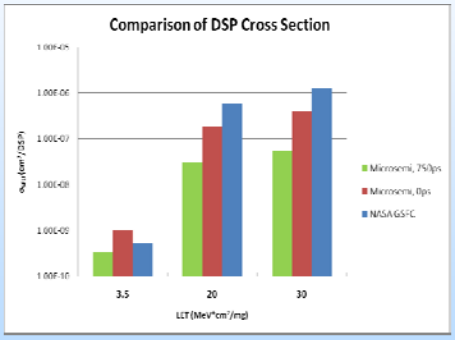
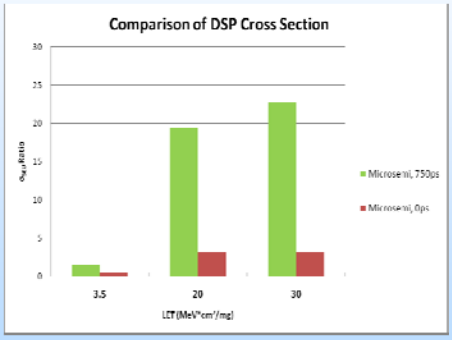
Result Comparison

- **Comparison of NASA REAG results with Microsemi results**





Source for Microsemi data: IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 57, NO. 6, DECEMBER 2010, pp. 3537-3546

Test Analysis

- **Cross sections show similar characteristics as results obtained by Rezgui et. Al., although appear 10X higher for case of multipliers at 120MHz with 750ps guard gate delay**
- **Surprisingly, cross sections more closely match results obtained by Rezgui et. Al. for case of multipliers at 120MHz with 0ps guard gate delay**
- **Are SETs effectively being filtered by delay chain of 750ps and guard-gate?**

Test Analysis

- **NASA REAG SEE Model for FPGAs**

$$P(fs)_{error} \propto P_{Configuration} + P(fs)_{functionalLogic} + P_{SEFI}$$

Probability for Design Specific system SEU: — *Probability for Configuration SEU* — *Probability for Functional logic SEU* — *Probability for Single Event Functional Interrupt*

- **For RTAX-DSP target device…**

$$P_{configuration} \to 0 \quad P_{SEFI} \to 0 \quad P_{DFFSEU} \to 0$$

$$P(f_s) \propto P(f_s)_{SET \to SEU} \propto \sum_{i=1}^{41} P_{gen}(i) \times P_{prop}(i) \times \tau_{width}(i) \times f_s$$

Test Analysis

- **Test results show that model is satisfied**
  - **As frequency increases, transients more likely to be captured within setup-hold time window around clock edge**

$$f_s \uparrow \Rightarrow P(f_s) \uparrow$$

  - **Higher LETs imply transients more likely to propagate thru several levels of combinatorial logic to output registers**

$$LET \uparrow \Rightarrow P_{prop} \uparrow \Rightarrow P(f_s) \uparrow$$

  - **Higher LETs imply transients more likely to be generated within combinatorial logic of DSP block**

$$LET \uparrow \Rightarrow P_{gen} \uparrow \Rightarrow P(f_s) \uparrow$$

- **Threshold LET seems higher than expected with SET mitigation via filtration by delay chain and guard gate design**

Next Steps

- Future testing to validate expected cross section saturation and threshold LET
- May limit testing to worst-case conditions (120 MHz) to increase data points
- Test at higher LETs to gather more data points and to observe if any potential DSP functional interrupts or global functional interrupts
- Test at all other input conditions (A_i, B_i coefficients set static instead of dynamic)

Acknowledgements/Closing

- RTAX-DSP FPGA devices remain good choice for designers of DSP algorithms targeting FPGAs for space
- All upsets observed appear to stem from transient capture at output registers of DSP cores
- I'd like to thank Melanie Berg, Mark Friendlich, Hak Kim for their expertise, assistance during test planning, design, execution, and analysis
- Questions?